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Development of ultra-fast ASIC for future PET scanners using TOF-capable MPPC detectors

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ABSTRACT

We have developed a front-end ASIC (MPPC32) intended for future PET scanners that offers time-of-flight (TOF) capability in conjunction with a multi-pixel photon counter (MPPC) array. The ASIC design is based on the open-IP project proposed by JAXA and was realized in TSMC 0.35-μm CMOS technology. The circuit comprises 32-channel, low impedance CMOS current conveyors (CCs) to effectively acquire fast MPPC signals. In order to precisely measure the coincidence timing of 511 keV gamma rays, the leading-edge method was employed instead of conventional zero-crossing measurement to discriminate signals. As a result, we obtained time jitter and walk measurement of 67 ps (FWHM) and 98 ps (within 511 keV ± 20%), respectively. Moreover, excellent energy resolutions of 9.8% (662 keV; FWHM) and 10.5% (511 keV; FWHM) were obtained by utilizing a 3×3 mm^2 MPPC (of 50 μm pitch) coupled with a Ce-doped LYSO (Ce:LYSO) crystal $3 \times 3 \times 10$ mm^3 in size. We finally report on the TOF measurements, and demonstrate that the MPPC32 developed here can be a promising device for future TOF-PET scanners using the MPPC array.

1. Introduction

An avalanche photodiode (APD) was expected to be applied for time-of-flight (TOF) and magnetic resonance imaging (MRI)-PET [1]. The APD is a compact high-performance light sensor that is immune to magnetic fields [2,3]. Moreover, the prototype depth-of-interaction (DOI) detector with multiple APD pixels is now being proposed instead of position-sensitive photomultiplier tubes (PMTs) [4].

For an initial study of novel PET detectors, we developed APD-based PET modules with high spatial resolution. The detector module consists of a large area APD array coupled one-to-one with a Ce-doped LYSO (Ce:LYSO) scintillator matrix and analog front-end cards in a compact size of $30 \times 30 \times 80$ mm^3. An image of the ^{22}Na source was reconstructed using the filtered back projection (FBP) algorithm. Thus, the high spatial resolutions of 0.9 mm (center; FWHM) and 1.3 mm (5.0 mm off axis; FWHM) were achieved [1]. However, time performance achieved a result no better than 3.1 ns (time jitter; FWHM) due to the limited frequency bandwidth of a charge sensitive amplifier (CSA) including a shaping circuit.

In order to improve the timing resolution, a multi-pixel photon counter (MPPC) has been applied for next-generation PET detectors [5,6]. Given the MPPC's high gain comparable to that of the PMT ($\sim 10^{5-6}$), a simple signal processing circuit can be constructed without a low-noise amplifier like the CSA that degrades time performance [7]. On the other hand, the MPPC's large capacitance (~ 300 pF) originates from the arrangement of micro APD-cell structures. The conventional input circuits used for other devices are consequently not available for fast signal processing involving the MPPC. This motivated us to develop an analog front-end ASIC (the MPPC32) optimized for MPPC readout. All circuit architectures of the MPPC32 are based on the open-IP LSI project led by JAXA. We successfully developed circuitry capable of excellent timing resolution.

In this paper, Section 2 describes the circuit architecture of the MPPC32. Sections 3 and 4 describe the experimental set-up and test results, respectively. And Section 5 presents our final conclusions.

2. Circuit architecture

2.1. Overview of MPPC32 design

The MPPC32 was implemented using TSMC 0.35-μm CMOS technology and was encapsulated in a 160-pin ceramic quad flat

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package (QFP) as shown in Fig. 1(a). Fig. 1(b) shows the chip layout. The chip is 3.3×7.5 mm^2 in size with 32-channel readout, and with maximum power dissipation of 500 mW in the entire chip for power rails of ± 1.65 V. Table 1 lists an overview of the ASIC parameters.

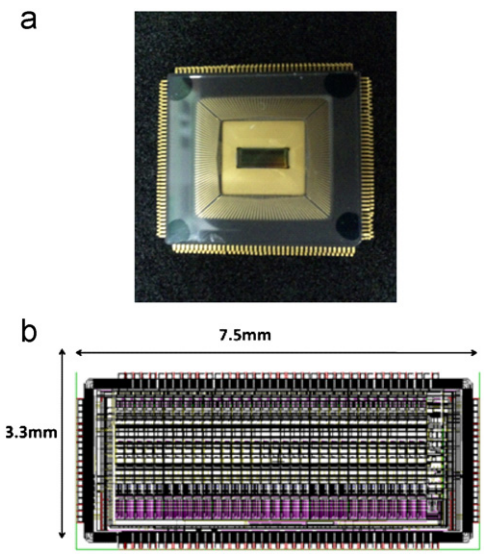

Fig. 1. (a) Photo of 160-pin ceramic QFP containing a bare chip. (b) The chip is 3.3×7.5 mm^2 in size with 32-channel MPPCs readout.

Table 1
Overview of the MPPC32 parameters.

Fabrication process	TSMC 0.35−μm CMOS
Chip size	3.3×7.5 mm^2
Package	160-pin Ceramic QFP
Number of channels	32
Operational input charge	200 pC @511 keV
Total power consumption	500 mW
Power rail	± 1.65 V

Fig. 2 shows the circuit diagram. The chip consists of two different systems (CHAIN1 and CHAIN2). We employed 32-channel CHAIN1s and a one-channel CHAIN2 to be combined with a MPPC array. CHAIN1 consists of current conveyors (CCs), a 2nd order shaping circuit (SHAPER), differentiator, and comparators for the energy and timing discrimination circuits. In particular, timing can be measured by applying two independent methods the leading-edge method and zero-crossing method. CHAIN1 provides position information via a parallel-to-serial (P to S) converter. CHAIN2 consists of a bias circuit, analog summing circuit (ASUM), monitor out selector, and two channels of time-to-amplitude converters (TACs) that provide energy and timing information via ASUM and TACs, respectively. The MPPC32 is also equipped with 30-bit local control registers (LCRs) and a 13-bit central control register (CCR) to adjust various parameters, including the baselines and amplitudes of analog signals.

2.2. Signal processing

The signal processing circuit of a MPPC must have low input impedance due to the MPPC's large capacitance. We employed a CC with impedance of 10 Ω to transfer signal charges fast to sequencing circuits. The CC is a current-mode analog circuit offering a wide dynamic range and a broad frequency range of operation, while a CMOS type CC enables higher circuit speed and lower power dissipation [8]. We developed the CC as implemented in CMOS technology based on the proposed ICON circuit cited in Ref. [9], and constructed the circuit without resistive feedback. Moreover, we equipped useful functions to cancel leakage current from internal circuits and compensate for intrinsic MPPC gain dispersion by controlling the amount of signal current.

CCs send 8/128 of the entire input charges to ASUM and SHAPER, and all of the rest to a leading-edge discriminator. SHAPER is a 2nd order low-pass filter used in shaping a CC output signal to semi-Gaussian. To make full use of the fast decay time characteristic of a Ce:LYSO scintillator (~ 40 ns), the shaping time constant was set to 64 ns.

ASUM sums all 32-channel outputs of the CCs, and also shapes via a 2nd order low-pass filter with a shaping time constant of 64 ns. The output of this circuit is connected to an external ADC, which provides an energy spectrum.

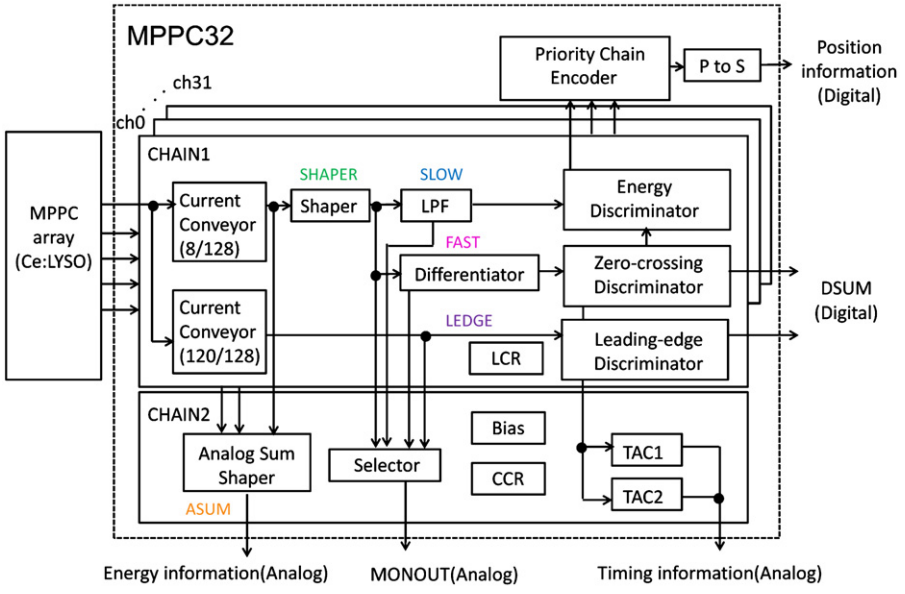

Fig. 2. Circuit diagram of the MPPC32. Two different systems (CHAIN1 and CHAIN2) coexist.

An energy discriminator circuit consists of four comparators. The first is a leading-edge discriminator used for the output of a low-pass filter (SLOW) having a low threshold as permitted by the noise level ($\sim$2% of 511 keV; rms), and enables the other comparators. The second and third comparators function as the lower and upper thresholds of an energy window. When the energy window holds an event of about 511 keV, a priority chain encoder outputs an 8-bit ID representing a MPPC pixel address via a parallel-to-serial converter. The last comparator is used for the zero-crossing discriminator described in Section 2.3 below.

2.3. Time measurement techniques

The zero-crossing and leading-edge methods are employed for the MPPC32. The zero-crossing method acquires the FAST signal, that is, the differentiating signal of SLOW. The zero-crossing discriminator outputs a hit timing signal (DSUM) as soon as a FAST signal crosses the zero point corresponding to SLOW signal peak. This technique was also used for other APD-ASICs (TIPPET08, TIPPET32). The references cited in Refs. [1,10] have demonstrated the time performance using the zero-crossing method. In contrast, the leading-edge method capture any fast initial rise of a large output signal of the CCs (LEDGE) at a certain threshold. Thus, a constant timing DSUM signal could be acquired without a time-walk free technique like constant fraction discriminator. We newly introduced the leading-edge method, and evaluated time performance in this paper. In practice, a SPICE simulation expects time performance to be 34 ps (time jitter; FWHM) and 71 ps (time walk; within 511 keV $\pm$ 20%) at a threshold set to 1.5% of 511 keV.

The DSUM signal commonly activates the two TACs with 50 ns set between each stop timing, and then the difference between both TAC amplitudes provides an event-by-event calibration scheme for the TAC circuit [10].

3. Experimental setup

The experimental setup was constructed to measure the energy spectrum and time resolution of the MPPC32, as coupled to a MPPC detector and pixelized scintillator. The MPPC32 was mounted on a socket connected to a testing board shown in Fig. 3. The testing board was also placed in a light-shielded aluminum box and regulated using a constant temperature reservoir. At testing board input, we attached a 3×3 mm^2 MPPC pixel whose Geiger-mode APDs were arranged with a pitch of 50 μm (Hamamatsu S10362-33-050C) coupled with a Ce:LYSO crystal $3\times3\times10$ mm^3 in size. All results in this paper were taken at 20 °C where the MPPC gain shows 7.5×10^5 at a bias voltage of 70.7 V. LabVIEW software (National Instruments LabVIEW 8.5 FPGA module) and the DAQ board (National Instruments PCI-7833R) featuring a built-in reconfigurable FPGA were used to control the setup. Digital signal readout, channel selection, amount of signal current, and offset equalization were controlled via an interface established by the software.

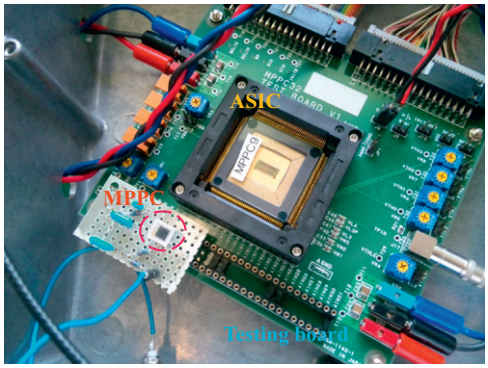

Fig. 3. Photo of testing board on which the MPPC32 and MPPC pixel are mounted.

4. Test results

4.1. Analog output waveforms

Fig. 4 (top) shows waveforms taken by a digital scope (Tektronix TDS 3034B) when the MPPC generated charges for 511 keV. The initial rise of LEDGE and the shaping time constants of other traces differ slightly from the simulation results shown in Fig. 4 (bottom), due to the slew rate of an analog buffer set between the testing board and digital scope. However, the experimental waveforms were considerably consistent with the simulation results. Moreover, the gain dispersion and offset voltages were within adjustable ranges.

4.2. Energy spectra

We obtained the energy spectra of the MPPC as coupled with the Ce:LYSO crystal using optical grease, via the MPPC32 ASIC developed in this paper. To acquire the related energy information, a voltage amplifier was used to amplify ASUM signals by a

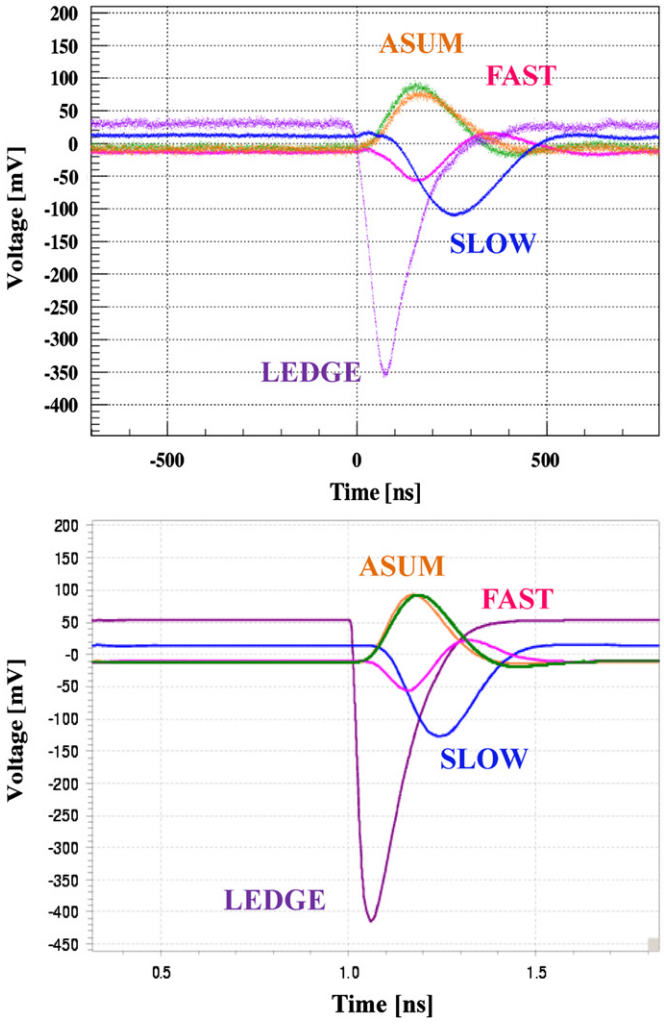

Fig. 4. (top) Experimental and (bottom) simulation output results for 511 keV.

factor of 10, followed by conversion into digital data by a 10-bit peak-hold ADC (Clear Pulse CP1114A). Ref. [7] describes how abundant incident photons from a Ce:LYSO crystal will cause a substantial non-linear MPPC response when irradiating high-energy gamma rays such as 662 keV. To calibrate the energy and relation with the output ADC channel, functional dependence was measured beforehand using various gamma-ray sources (^{22}Na,^{57}Co,^{137}Cs, and ^{241}Am). Fig. 5 presents the energy spectra of ^{137}Cs (blue dotted plots) and ^{22}Na (red dotted plots). The energy resolutions for 662 keV and 511 keV were 9.8% (FWHM) and 10.5% (FWHM), respectively.

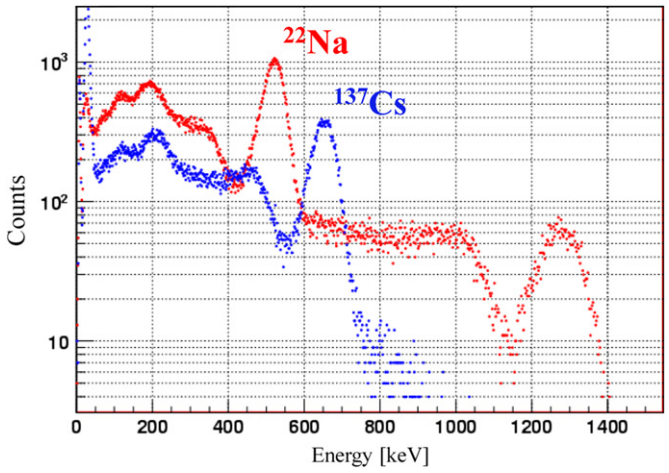

Fig. 5. Energy spectra of ^{137}Cs (blue dotted plot) and ^{22}Na (red dotted plot) sources. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

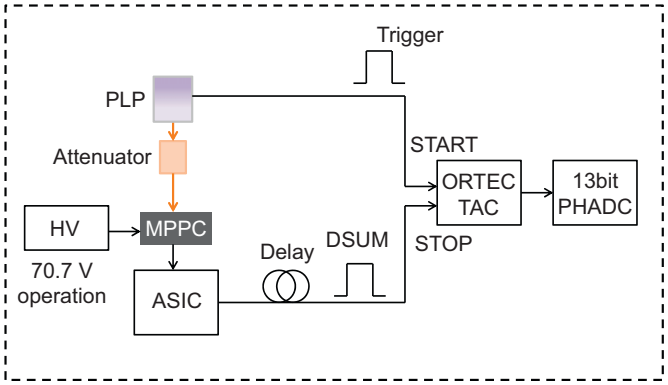

Fig. 6. Diagram of time walk and jitter measurement. A pico-second 655-nm laser was used to irradiate the MPPC.

4.3. Time jitter and walk measurements

To check the fast time response of the MPPC32, time resolution was measured with the MPPC irradiating a laser pulse. We used a pico second light pulsar (PLP; Hamamatsu M10306-02) to acquire fast MPPC signals, where a fast rise time of 7 ns and a decay time of 38 ns were observed by the digital scope with 50 Ω termination. Fig. 6 shows a diagram of the setup for measuring time performance. The MPPC was illuminated by a 655-nm laser with a pulse duration of 54 ps (FWHM) at 1-kHz repetition, while the PLP output a NIM logic trigger synchronized with a pulse. The output laser was guided to an optical attenuator (ANDO AQ-1227) with glass fiber and attenuated within 0–16 dB. The laser intensity was calibrated to match the light output of Ce:LYSO when irradiating a 511 keV gamma ray in advance. The light intensity was also varied within the light output equivalent to 511 keV ± 20% during walk measurement. We measured the hit timing using the leading-edge method, and also input DSUM signals to an external TAC module (ORTEC 567). Moreover, we obtained the timing spectra via a 13-bit ADC (Clear Pulse CP1114A) by referring to the PLP output trigger. The results were 67 ps (time jitter; FWHM) and 98 ps (time walk; within 511 keV ± 20%) at a threshold set to 10% of 511 keV.

4.4. TOF experiment

Finally, a coincidence experiment involving two MPPCs was conducted by measuring the timing spectra, thereby reflecting TOF information. Fig. 7 shows a detailed diagram of the setup. The two MPPC32 testing boards attached the MPPC coupled with the Ce:LYSO crystal were set with a ^{22}Na source placed at one of two different positions ("A" or "B") spaced 80 mm apart. Each DSUM signal processed using the leading-edge method was input to the external TAC module and digitalized by the 13-bit ADC, while ASUM signals were discriminated by two external discriminators (Technoland N-TM 210V4). Each energy window was set within 511 keV ± 20%, with a gate signal being output to the ADC when the window held an event of a 511 keV annihilation gamma ray.

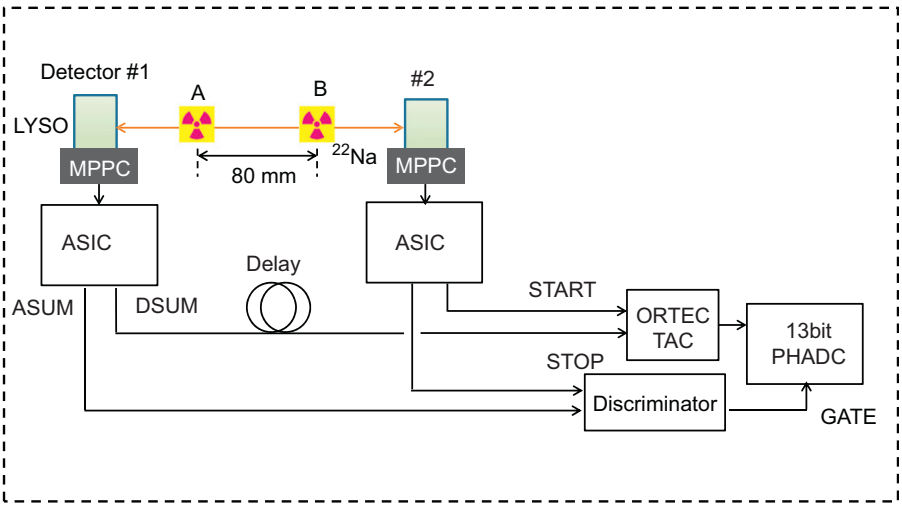

Fig. 7. Diagram of the TOF experiment. A ^{22}Na source was set at one of two different positions ("A" or "B") spaced 80 mm apart.

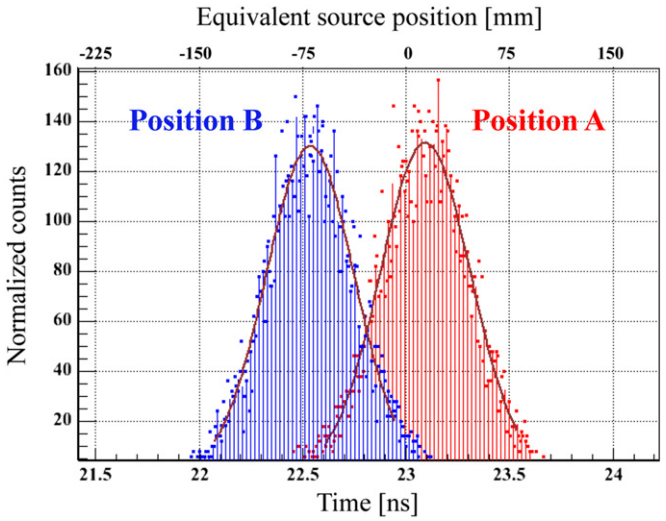

Fig. 8. Timing spectra reflecting TOF information. The timing spectra were clearly resolved above FWHM. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

Fig. 8 shows the timing spectra at both positions (A, red plot; B, blue plot). The average coincidence time resolution of the spectra was 491 ps (FWHM), which corresponds to 74-mm TOF position resolution; moreover, the result revealed that both spectra were clearly resolved above FWHM. Moreover, the 540-ps difference between the spectrum peaks properly reflected the TOF position information.

5. Conclusions

In this work, we developed an analog front-end ASIC (MPPC32) optimized for MPPC readout to improve the time performance of PET modules. We tested chip performance together with a 3×3 mm^2 MPPC (of 50 μm pitch) and a Ce:LYSO crystal $3 \times 3 \times 10$ mm^3 in size. Excellent energy resolutions of 9.8% (662 keV; FWHM) and 10.5% (511 keV; FWHM) were obtained. We also measured time jitter and walk resolution, obtaining the results of 67 ps (time jitter; FWHM) and 98 ps (time walk; within 511 keV $\pm$ 20%) with a threshold set to 10% of 511 keV. Moreover, the coincidence timing resolution between two MPPCs was 491 ps (FWHM), when timing spectra were clearly resolved above FWHM by a ^{22}Na source at positions spaced 80 mm apart. These results suggest that the MPPC32 in collaboration with a MPPC could be a promising device for future TOF-PET scanners.

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